What is claimed is:

1. A phase-interpolation circuit for outputting a third clock signal according to a first clock signal and a second clock signal, the circuit comprising:

a first inverter for receiving the first clock signal;

a second inverter for receiving the second clock signal, wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal;

a first controlled switch coupled to the first inverter, the second inverter, and a power source, wherein the first controlled switch being "off" when the first clock signal is in a fist state, and being "on" when the first clock signal is in a second state; and

a second controlled switch coupled to the first inverter, the second inverter, and ground, wherein the second controlled switch being "on" when the first clock signal is in the first state, and being "off" when the first clock signal is in the second state;

wherein the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal;

wherein the first controlled switch and the second controlled switch are to

avoid a short-circuit current of the phase-interpolation circuit.

2. The phase-interpolation circuit of claim 1, wherein the circuit further comprises a third inverter coupled to the common output end to output the third clock signal.

3. The phase-interpolation circuit of claim 1, wherein the circuit further comprises:

a fourth inverter to output the first clock signal to the first inverter; and

a fifth inverter to output the second clock signal to the second inverter.

4. The phase-interpolation circuit of claim 1, wherein the first controlled switch comprises:

a first PMOS coupled between the first inverter and the power source, the first PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state; and

a second PMOS coupled between the second inverter and the power source, the second PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state.

5. The phase-interpolation circuit of claim 1, wherein the second controlled

switch comprises:

a first NMOS coupled between the first inverter and the ground, the first NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state; and

a second NMOS coupled between the second inverter and the ground, the second NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state.

6. The phase-interpolation circuit of claim 1, wherein the first controlled switch at least includes a PMOS.

7. The phase-interpolation circuit of claim 1, wherein the second controlled switch at least includes a NMOS.

8. The phase-interpolation circuit of claim 1, wherein the first and the second inverter are CMOS inverters.

9. A phase-interpolation circuit for outputting a third clock signal according to a first clock signal and a second clock signal, the circuit comprising:

a first inverter for receiving the first clock signal;

a second inverter for receiving the second clock signal, wherein an output

end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal;

a first controlled switch coupled to the first inverter, the second inverter, and a power source, wherein the first controlled switch being "off" when the first clock signal is in a fist state, and being "on" when the first clock signal is in a second state; and

a second controlled switch coupled to the first inverter, the second inverter, and ground, wherein the second controlled switch being "on" when the first clock signal is in the first state, and being "off" when the first clock signal is in the second state;

wherein the first controlled switch and the second controlled switch are to avoid a short-circuit current of the phase-interpolation circuit.

10. The phase-interpolation circuit of claim 9, wherein the circuit further comprises a third inverter coupled to the common output end to output the third clock signal.

11. The phase-interpolation circuit of claim 9, wherein the circuit further comprises:

a fourth inverter to output the first clock signal to the first inverter; and

a fifth inverter to output the second clock signal to the second inverter.

12. The phase-interpolation circuit of claim 9, wherein the first controlled switch comprises:

a first PMOS coupled between the first inverter and the power source, the first PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state; and

a second PMOS coupled between the second inverter and the power source, the second PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state.

13. The phase-interpolation circuit of claim 9, wherein the second controlled switch comprises:

a first NMOS coupled between the first inverter and the ground, the first NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state; and

a second NMOS coupled between the second inverter and the ground, the second NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state.

14. The phase-interpolation circuit of claim 9, wherein the first controlled

switch at least includes a PMOS.

15. The phase-interpolation circuit of claim 9, wherein the second controlled switch at least includes a NMOS.

16. The phase-interpolation circuit of claim 9, wherein the first and the second inverter are CMOS inverters.